Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] A method of fabricating a transistor, the method comprising the steps of:

forming an emitter landing pad over a first extrinsic base layer, the first extrinsic base layer being above an intrinsic base;

forming an opening to the first extrinsic base layer, the opening generating a remaining portion of the landing pad to a side of the opening;

oxidizing to form an oxide region in a portion of the first extrinsic base layer, the oxide region including an oxide section extending below a portion of the remaining portion;

removing the oxide region within the opening and leaving the oxide section; and

using the oxide section to determine a spacing between an emitter formed in the opening and the first extrinsic base layer.

[c2] The method of claim 1, further comprising the step of forming the first extrinsic base layer by depositing a polysilicon layer upon the intrinsic base to a predefined thickness.

[c3] The method of claim 1, further comprising the step of forming the first extrinsic base layer by epitaxially growing a silicon layer upon the intrinsic base to a predefined thickness.

[c4] The method of claim 1, further comprising the step of forming a spacer in the opening after the oxidizing step.

[c5] The method of claim 1, further comprising the step of forming a spacer in the opening prior to the oxidizing step.

[c6] The method of claim 1, wherein the using step includes depositing an emitter polysilicon in the opening to form the emitter.

[c7] The method of claim 6, wherein the emitter extends under a portion of a spacer formed in the opening.

[c8] A transistor comprising:
a remaining portion of an emitter landing pad that is distanced from an intrinsic base.

[c9] The transistor of claim 8, wherein the remaining portion is distanced from the intrinsic base by an extrinsic base layer, and the extrinsic base layer includes an oxide section that determines a distance between an emitter and an extrinsic base.

[c10] The transistor of claim 9, wherein a width of the oxide section determines a base resistance.

[c11] The transistor of claim 10, wherein the width of the oxide section determines a length of the remaining portion that current must traverse as current passes through the extrinsic base.

[c12] The transistor of claim 11, wherein the thickness of the oxide section is sufficient to prevent current from having to traverse the remaining portion.

[c13] A transistor comprising:

an emitter;

a first extrinsic base layer;

a second extrinsic base layer electrically connected to the first extrinsic base layer;

an oxide section in the first extrinsic base layer adjacent the emitter; and

a remaining portion of an emitter landing pad that separates each of the first and second extrinsic base layer from one another adjacent the emitter.

[c14] The transistor of claim 13, wherein the extrinsic base includes the first extrinsic base layer and a second extrinsic base layer, and the first extrinsic base layer is doped at a different concentration than the second extrinsic

base layer.

[c15] The transistor of claim 14, wherein the oxide section is positioned within the first extrinsic base layer.

[c16] The transistor of claim 14, wherein the first extrinsic base layer includes a first region including a doped silicon and a second region includes a doped polysilicon, and the oxide section is in the first region.

[c17] The transistor of claim 13, further comprising a remaining portion of an emitter landing pad positioned above the oxide section.

[c18] The transistor of claim 13, wherein a width of the oxide section determines a base resistance.

[c19] The transistor of claim 18, wherein the width of the oxide section determines a length of the remaining portion that current must traverse as the current passes through the extrinsic base.

[c20] The transistor of claim 19, wherein the thickness of the oxide section is sufficient to prevent the current from having to traverse the remaining portion.

[c21] The transistor of claim 13, wherein the emitter extends under a portion of a spacer.

[c22] The transistor of claim 13, wherein the first and second extrinsic base layers extend in a horizontally overlapped fashion from the emitter to a common edge.

[c23] A transistor comprising:
an emitter extending through a remaining portion of an emitter landing pad to an intrinsic base; and
an oxide section in an extrinsic base layer, the oxide portion extending below a part of the remaining portion, wherein a width of the oxide section determines an amount of base resistance.

[c24] The transistor of claim 23, wherein the thickness determines a length of the remaining portion that current must traverse as the current passes through an extrinsic base.

[c25] The transistor of claim 23, wherein the extrinsic base layer extends under another part of the remaining portion and elevates the remaining portion from the intrinsic base.

[c26] The transistor of claim 25, wherein the extrinsic base includes a first layer and a second layer, and the oxide section is positioned within the first layer, and the first layer includes a first region including a doped silicon and a second region including a doped polysilicon.

[c27] A method of fabricating a transistor, the method comprising the steps of:
embedding an emitter landing pad in an extrinsic base such that the emitter landing pad is distanced from an intrinsic base;
forming an opening through the emitter landing pad leaving a remaining portion of the emitter landing pad;
forming an oxide section below the remaining portion;
and
forming an emitter in the opening such that the emitter extends to the intrinsic base.

[c28] The method of claim 27, wherein the embedding step includes forming a first extrinsic base layer by depositing a doped polysilicon layer upon the intrinsic base to a predefined thickness, forming the emitter landing pad and depositing a second extrinsic base layer.

[c29] The method of claim 27, wherein the embedding step includes forming the first extrinsic base layer by epitaxially growing a doped silicon layer upon the intrinsic base to a predefined thickness, forming the emitter landing pad and depositing a second extrinsic base layer.

[c30] The method of claim 27, wherein the step of forming an oxide section includes depositing an oxide layer in the

opening.